EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	53	703/22.ccls. and @pd>"20080101"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/02 10:58
L2	22	(golden adj reference) and (hdl or verilog or vhdl or rtl) and @ad<"20031001"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/02 11:09
L3	9	(pli or (program$4 adj language adj interface$1)) and (ISS or (instruction adj set adj simulat$5)) and (rtl or hdl or verilog or vhdl) and @ad<"20031001"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/02 11:13

EAST Search History

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L4	1	((simulation adj design) and (reference adj value)).clm.	US-PGPUB	OR	OFF	2008/07/02 11:37
L5	0	((programming adj language adj interface) and (reference adj value)).clm.	US-PGPUB	OR	OFF	2008/07/02 11:38
L6	0	((PLI) and (reference adj value)).clm.	US-PGPUB	OR	OFF	2008/07/02 11:38

Results for "((iss<and>pli)<and>(hdl or verilog or rtl or vhdl)) <and> (pyr >= 1913 <and&..."
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» Key

IEEE JNL	IEEE Journal or Magazine
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IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

1. **Software development in a hardware simulation environment**
   Schnaider, B.; Yogev, E.;
   Design Automation Conference Proceedings 1996, 33rd
   3-7 June 1996 Page(s):684 - 689
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2. **Core design and system-on-a-chip integration**
   Rincon, A.M.; Cherichetti, G.; Monzel, J.A.; Stauffer, D.R.; Trick, M.T.;
   Design & Test of Computers, IEEE
   Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):26 - 35
   Digital Object Identifier 10.1109/54.632878
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3. **A dynamic random instruction and stimulus generation for functional ve processor**
   Liang Zhongshu; Yan Xiaolang; Wang Jiebing; Xu Zhihan;
   ASIC, 2003. Proceedings. 5th International Conference on
   Volume 1, 21-24 Oct. 2003 Page(s):459 - 462 Vol.1
   Digital Object Identifier 10.1109/ICASIC.2003.1277585
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4. **A hardware-software co-simulator for embedded system design and del**
   Ghosh, A.; Bershteyn, M.; Casley, R.; Chien, C.; Jain, A.; Lipsie, M.; Tarroday
   Design Automation Conference, 1995. Proceedings of the ASP-DAC '95/CHC International Conference on Hardware Description Languages; IFIP Internatic Large Scale Integration., Asian and South Pacific
   29 Aug.-1 Sept. 1995 Page(s):155 - 164
   Digital Object Identifier 10.1109/ASPDAC.1995.486217
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... In the environment, **ISS** and **HDL** simulator communicate ... is built using the standard IPC library and the Verilog Program Language Interface(**PLI**) li- brary. ...
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W Yang, MK Chung, CM Kyung - SOC Conference, 2003. Proceedings. IEEE International [..., 2003 - ieeexplore.ieee.org
... using suitable interfaces such as **PLI**, VPI, FLI ... integration with existing **HDL** design tools and flexible API ... set simulafor (IS$J Interpretive **ISS** executes the ...
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... C' Instruction Set Simulators (**ISS**) fre- quently ... language" **VHDL** attributes (or **PLI** for Verilog). ... Comparatively to full **HDL** models, distributed models ...
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... built using the standard IPC library and the **Verilog** Program Language Interface(**PLI**) li- brary. ... tion for consistency checking from the **ISS** and adjusts ...
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B Schnaider, E Yogev - Annual ACM IEEE Design Automation Conference: Proceedings of ..., 1996 - doi.ieeecomputersociety.org
... in "C" and implemented as a **PLI** code which is ... It is implemented as a **Verilog** stub which is ... the API to the target processor instruction set simulator (**ISS**). ...
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... and industry standard tools such as **Verilog** and VHDL ... generators, peripherals, and system memory through **PLI** calls ... **ISS** Coverage Coverage Target AVP+MVP RTPG VSG ...
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... Synchronization between different **verification** engines (netlist, RTL, or **ISS** simulators and ... **PLI** provides a mecha- nism to interface **Verilog** programs with ...
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... language using suitable interfaces such as **PLI**, VPI, FLI ... enhance the performance of the **ISS**, compiled code ... existing languages in academia, with **Verilog** and VHDL ...
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... Dynamic Random Insti-uction Generation (DRIG), **PLI**, DUT. Instniction Set Simulator (**ISS**) I Introduction The complexity of ... as the input to both the **RTL** and the ...
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... Another approach allows debugging in **RTL** while running gate ... using suitable interfaces such as **PLI**, VPI, FLI ... set simulafor (IS§J Interpretive **ISS** executes the ...
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